## I. Claim Rejections - 35 USC §102

### 1. Rejection Under §102(e) Over Zhang et al.

In the Final Rejection, the Examiner rejects Claims 40, 44 and 45 under 35 USC §102(e) as being anticipated by Zhang et al. In the Advisory Action, the Examiner maintained this rejection and stated:

> "Claim 40 does not distinguish over the Zhang et al. reference because Zhang et al. clearly discloses the second wiring 311 connected to the TFT through a contact hole in a first insulating layer 315. Note that without a contact hole in the first insulating layer 315, the second wiring 311 cannot be connected to the TFT."

This rejection is respectfully traversed, as discussed below.

Independent Claim 40 has now been amended to recite that "said second wiring is directly connected to said semiconductor layer though a contact hole provided in said first insulating film." This clearly distinguishes the claimed invention from Zhang. More specifically, Fig. 3B of Zhang, which was cited by the Examiner, discloses layer 311 (the alleged second wiring) *connected to* layer 310 (the alleged first wiring) through layer 315 (a second insulating layer). Layer 310 is then connected to the TFT through a contact hole in the first insulating layer. Hence, it does not disclose or suggest layer 311 or a second wiring *directly* connected to the TFT through a contact hole in layer 315.

This is in contrast to, for example, Fig. 3C of the present application wherein a first wiring 112 is formed over a first insulating film 111, and a second wiring 114 is formed over the first wiring 112 and is *directly* connected to the TFT through a contact hole in first insulating film 111.

Hence, amended independent Claim 40 and those claims dependent thereon are not disclosed or suggested by Zhang but are patentable thereover. Accordingly, it is requested that this rejection be withdrawn.

2. **Rejection Under §102(a) Over Yoon**

In the Final Rejection, the Examiner further rejected Claim 40 under 35 USC §102(a) as being anticipated by Yoon. In the Advisory Action, the Examiner stated:

> "Claim 40 does not distinguish over the Yoon reference since the claimed language does not state [sic that] a pixel electrode cannot be a bit line."

This rejection is also respectfully traversed, as discussed below.

In the Final Rejection, the Examiner alleges that Yoon discloses a pixel electrode 118 formed on a second insulating film. Yoon, however, defines 118 as a bit line (see e.g. col. 3, ln. 47). Applicants respectfully submit that one skilled in the art would not confuse a bit line and a pixel electrode. A pixel electrode is an electrode for driving a liquid crystal, an electroluminescence, etc. This is very different than a bit line which is a shared signal line used to connect all memory cell outputs of one column together as a shared line. (See attachment hereto defining "bit line" from Laplante, "Comprehensive Dictionary of Electrical Engineering", p. 63 (1999)). See also col. 1, lns. 33-37 of Yoon. Further, there also appears to be nothing in Yoon defining, disclosing or suggesting a pixel electrode.

There is no requirement (and the Examiner has cited no rule or law for such a requirement) that Applicants in their claims state that the claimed language cannot be something that one skilled in the art would never expect it to be. Such a requirement is senseless. Accordingly, it is requested that this rejection be withdrawn.

**RESPONSE TO OTHER ITEMS IN THE FINAL REJECTION**

In the Final Rejection, the Examiner had a number of other objections and rejections of the claims. As the Advisory Action gave no indication of the status of these objections and rejections, Applicants will again address each below.

## II. Claim Rejections - 35 USC §103

### 1. Rejection Under §103 Over Yoon In View Of Yamazaki

In the Final Rejection, the Examiner also rejected Claims 1-12, 19-24, 28-39 and 41-45 under 35 USC §103 as being unpatentable over Yoon in view of Yamazaki. This rejection is also respectfully traversed.

As explained above and contrary to the Examiner's assertion, 118 of Yoon is described as a bit line, not a pixel electrode. Further, there is no pixel electrode defined in Yoon.

Yamazaki discloses a pixel electrode 121 directly connected to drain region 111 (see Fig. 2B). It does not disclose a pixel electrode connected to a second metallic layer through a contact hole in a second insulating film, as recited in independent Claims 1, 7 (and similar language in independent Claims 19, 28 34).

Hence, even if these references are somehow combined, the combination still fails to disclose or suggest the structure of the independent claims, or those claims dependent thereon, of the present application. Therefore, it is requested that this rejection be withdrawn.

### 2. Rejection Under §103 Over Zhang et al. In View Of Yamazaki

The Examiner further rejected Claims 1-12, 19-24, 28-33 and 41-43 under 35 USC §103 as being unpatentable over Zhang et al. in view of Yamazaki. This rejection is also respectfully traversed.

As explained above, Zhang does not disclose or suggest a second metallic layer *directly* connected to a conductive layer at the bottom of a contact hole, as recited in amended independent Claim 1 (and similarly in the other amended independent claims). Yamazaki also does not appear to disclose such a structure. Hence, neither of these references disclose or suggest the claimed invention, and it is requested that the rejection be withdrawn.

## III. Claim Objections

The Examiner objected to informalities in Claims 41 and 42 and in particular, requested that "conductive" be changed to -- wiring -- . Applicants did so in Amendment C and request that this objection be withdrawn.

## IV. Claim Rejections - 35 USC §112

The Examiner also rejected Claim 43 under 35 USC §112 as being indefinite. In particular, the Examiner stated that "organic material" in Claim 43 lacks antecedent basis. Applicants amended Claim 43 in Amendment C to change "organic material is" to -- first insulating layer comprises-- . This should resolve the Examiner's rejection regarding lack of antecedent basis, and therefore, it is requested that this rejection be withdrawn.

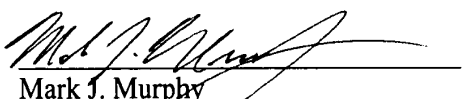
For at least the above-stated reasons, the device of the claims of the present application is not disclosed or suggested by the cited references, and the application is now in a condition for allowance. Therefore, it is requested that the application now be allowed.

Applicants do not believe that any further fee is due for this amendment. Please charge our Deposit Account No. 50-1039 for any deficiency.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: May 14, 2002



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Marked up copy of the claims as amended:

**IN THE CLAIMS:**

Please amend the claims as follows:

1. (Twice Amended) A semiconductor device comprising:

a first insulating film comprising an organic material formed over a conductive layer;

a first metallic layer formed on said first insulating film;

a second metallic layer formed on said first metallic layer;

a second insulating film formed on said second metallic layer; and

a pixel electrode formed on said second insulating film, said pixel electrode being connected to said second metallic layer through a contact hole provided in said second insulating film,

wherein said conductive layer and said second metallic layer are directly connected to each other at the bottom of a contact hole provided in said first insulating film.

7. (Twice Amended) A semiconductor device comprising:

a first insulating film comprising an organic material formed over a thin film transistor;

a first metallic layer formed on said first insulating film;

a second metallic layer formed on said first metallic layer;

a second insulating film formed on said second metallic layer; and

a pixel electrode formed on said second insulating film, said pixel electrode being connected to said second metallic layer through a contact hole provided in said second insulating film,

wherein a source region or a drain region of said thin film transistor and said second metallic layer are directly connected to each other at the bottom of a contact hole provided in said first insulating film.

19. (Twice Amended) A semiconductor device comprising:

a first insulating film comprising an organic material formed over a thin film transistor;

a first conductive layer formed on said first insulating film;

a second conductive layer formed on said first conductive layer;

a second insulating film formed on said second conductive layer; and

a pixel electrode formed on said second insulating film, said pixel electrode being connected to said second conductive layer through a contact hole provided in said second insulating film,

wherein a source region or a drain region and said second conductive layer are directly connected to each other at the bottom of a contact hole provided in said first insulating film,

wherein said second conductive layer is contact with said first insulating film inside of said contact holes.

28. (Twice Amended) A semiconductor device comprising:

a thin film transistor formed over a substrate, said thin film transistor having a semiconductor layer and a gate electrode adjacent to said semiconductor layer with a gate insulating film interposed therebetween;

a first insulating film comprising an organic material formed over said thin film transistor;

a first conductive layer formed on said first insulating film;

a second conductive layer formed on said first conductive layer;

a second insulating film formed on said second conductive layer; and

a pixel electrode formed on said second insulating film, said pixel electrode being connected to said second conductive layer through a contact hole provided in said second insulating film,

wherein said second conductive layer is directly connected to said semiconductor layer though a contact hole provided in said first insulating film.

34. (Twice Amended) A semiconductor device comprising:

a thin film transistor formed over a substrate, said thin film transistor having a semiconductor layer and a gate electrode adjacent to said semiconductor layer with a gate insulating film interposed therebetween;

a first insulating film comprising an organic material formed over said thin film transistor;

a first conductive layer formed on said first insulating film;

a second conductive layer formed on said first conductive layer;

a second insulating film formed on said second conductive layer; and

a pixel electrode formed on said second insulating film, said pixel electrode being connected to said second conductive layer through a contact hole provided in said second insulating film,

wherein said second conductive layer is directly connected to said semiconductor layer though a contact hole provided in said first conductive layer and said first insulating film.

40. (Amended) A semiconductor device comprising:

a thin film transistor formed over a substrate, said thin film transistor having a semiconductor layer and a gate electrode adjacent to said semiconductor layer with a gate insulating film interposed therebetween;

a first insulating film formed over said thin film transistor;

a first wiring formed on said first insulating film;

a second wiring formed on said first wiring;

a second insulating film formed on said second wiring; and

a pixel electrode formed on said second insulating film, said pixel electrode being connected to said second wiring through a contact hole provided in said second insulating film,

wherein said second wiring is directly connected to said semiconductor layer though a contact hole provided in said first insulating film.

target in the direction other than that of the illuminating source.

**bit** (1) the fundamental unit of information representation in a computer, short for "binary digit" and with two values usually represented by "0" and "1." Bits are usually aggregated into "bytes" (7 or 8 bits) or "words" (12–60 bits).

A single bit within a word may represent the coefficient of a power of 2 (in numbers), a logical TRUE/FALSE quantity (masks and Boolean quantities), or part of a character or other compound quantity. In practice, these uses are often confused and interchanged.

(2) in Information Theory, the unit of information. If an event $E$ occurs with a probability $P(E)$, it conveys information of $\log_2(1/P(E))$ binary units or bits. When a bit (binary digit) has equiprobable 0 and 1 values, it conveys exactly 1.0 bit (binary unit) of information; the average information is usually less than this.

**bit energy** the energy contained in an information-bearing signal received at a communications receiver per information bit. The power of an information bearing signal at a communications receiver divided by the information bit rate of the signal. Usually denoted by $E_b$ as in the signal to noise ratio $E_b/N_0$.

**bit error rate (BER)** the probability of a single transmitted bit being incorrectly determined upon reception.

**bit line** used in, for example, RAM memory devices (dynamic and static) to connect all memory cell outputs of one column together using a shared signal line. In static RAM, the "bit" line together with its complemented signal "-bit" feeds a "sense amplifier" (differential in this case) at the bottom of the column serving as a driver to the output stage. The actual cell driving the bit line (and -bit) is controlled via an access transistor in each cell. This transistor is turned on/off by a "word" line, a signal run across the cells in each row.

**bit parallel** a method to transmit or process information in which several bits are transmitted in parallel. Examples: a bit parallel adder with 4-bit data has 8 input ports for them (plus an initial carry bit); an 8-bit parallel port includes true 8-bit bi-directional data lines. (MP)

**bit per second (bps)** measure of transfer rate of a modem or a bus or any digital communication support. (*See also* baud and baud rate. bps and baud are not equivalent since bps is a low-level measure and media; thus, it includes the number of bits sent for the low-level protocol, while baud is typically referred to a higher level of transmission).

**bit period** the time between successive bits in data transmission or data recording. At the transmitter (or recorder) the timing is established by a clock. At the receiver (or reader) an equivalent clock must be recovered from the bit stream.

**bit plane** the binary $N \times N$ image formed by selecting the same bit position of the pixels when the pixels of an $N \times N$ image are represented using $k$ bits.

**bit plane encoding** lossless binary encoding of the bit planes is termed bit plane encoding. The image is decomposed into a set of $k$, $N \times N$ bit planes from the least significant bit to $k-1$ most significant bits and then encoded for image compression.

**bit rate** a measure of signaling speed; the number of bits transmitted per second. Bit rate and baud are related but not identical. Bit rate is equal to baud times the number of bits used to represent a line state. For example, if there are sixteen line states, each line state encodes four bits, and the bit rate is thus four times the baud. *See also* baud.